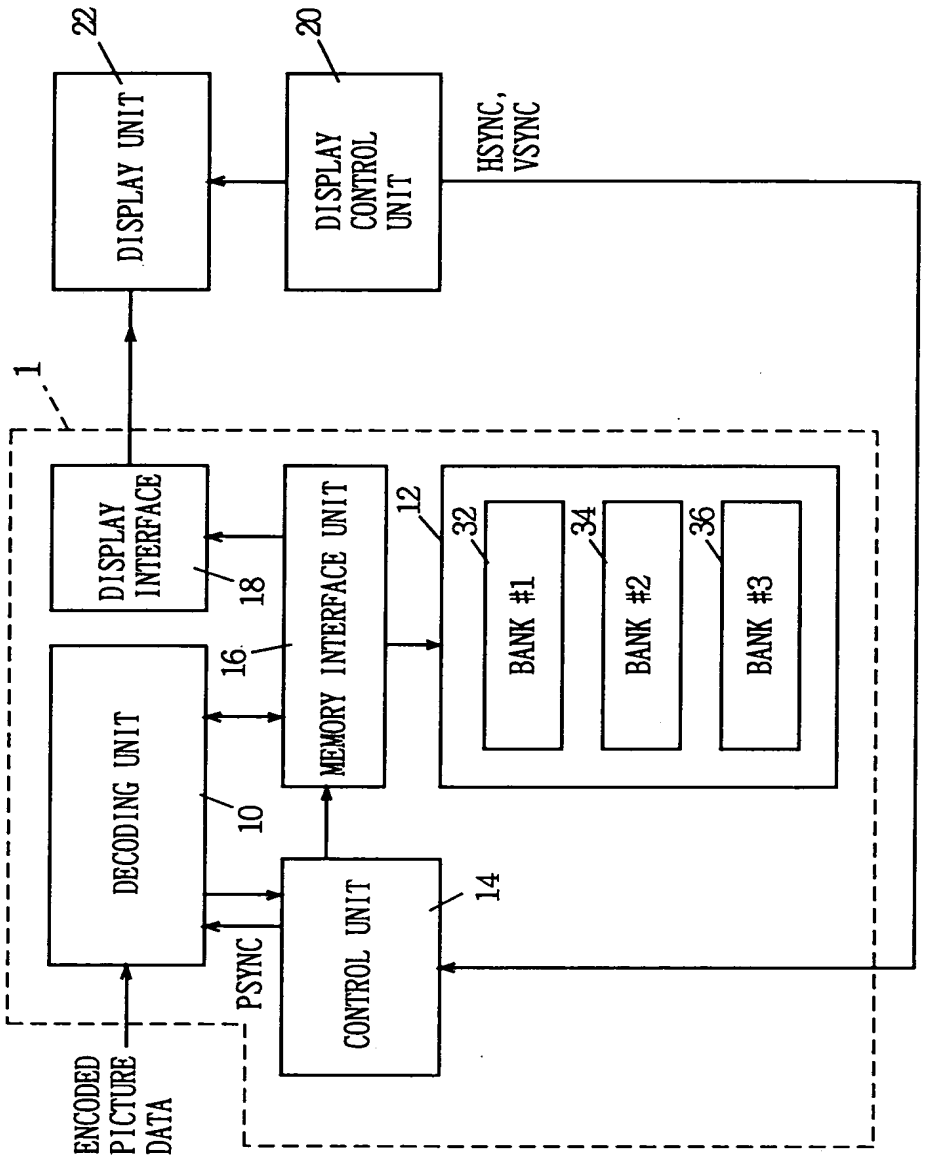
O.G. Fig.
CLASS
BY

FIG. 1



Figs. 44

O.G. FIG. CLASS SUBCLASS BY DRAFTSMAN

FIG. 2A

DISPLAY ORDER OF RESPECTIVE FRAMES

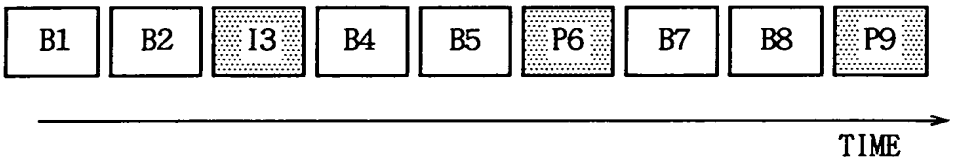


FIG. 2B

DECODING ORDER OF RESPECTIVE FRAMES (ORDER IN ENCODED DATA)

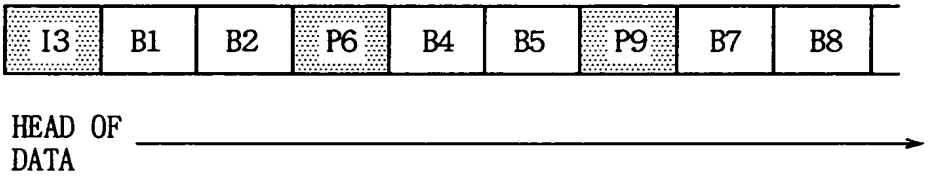
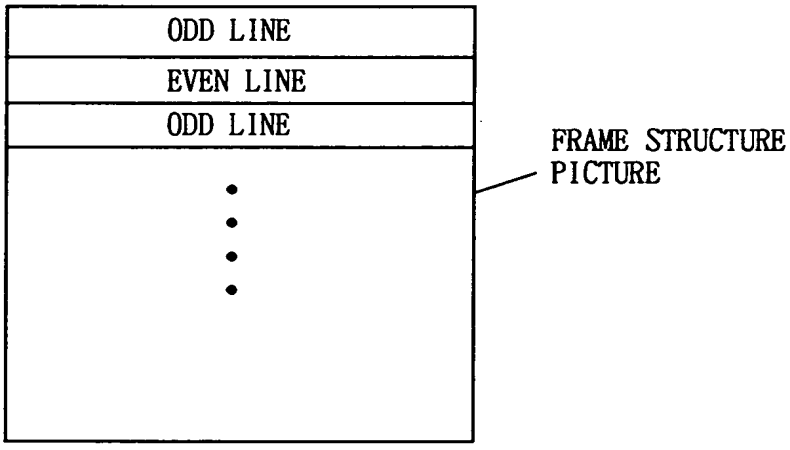


FIG. 3



O.G. FIG.
BY
CLAS. SUBCLASS
DRAFTSMAN

FIG. 4

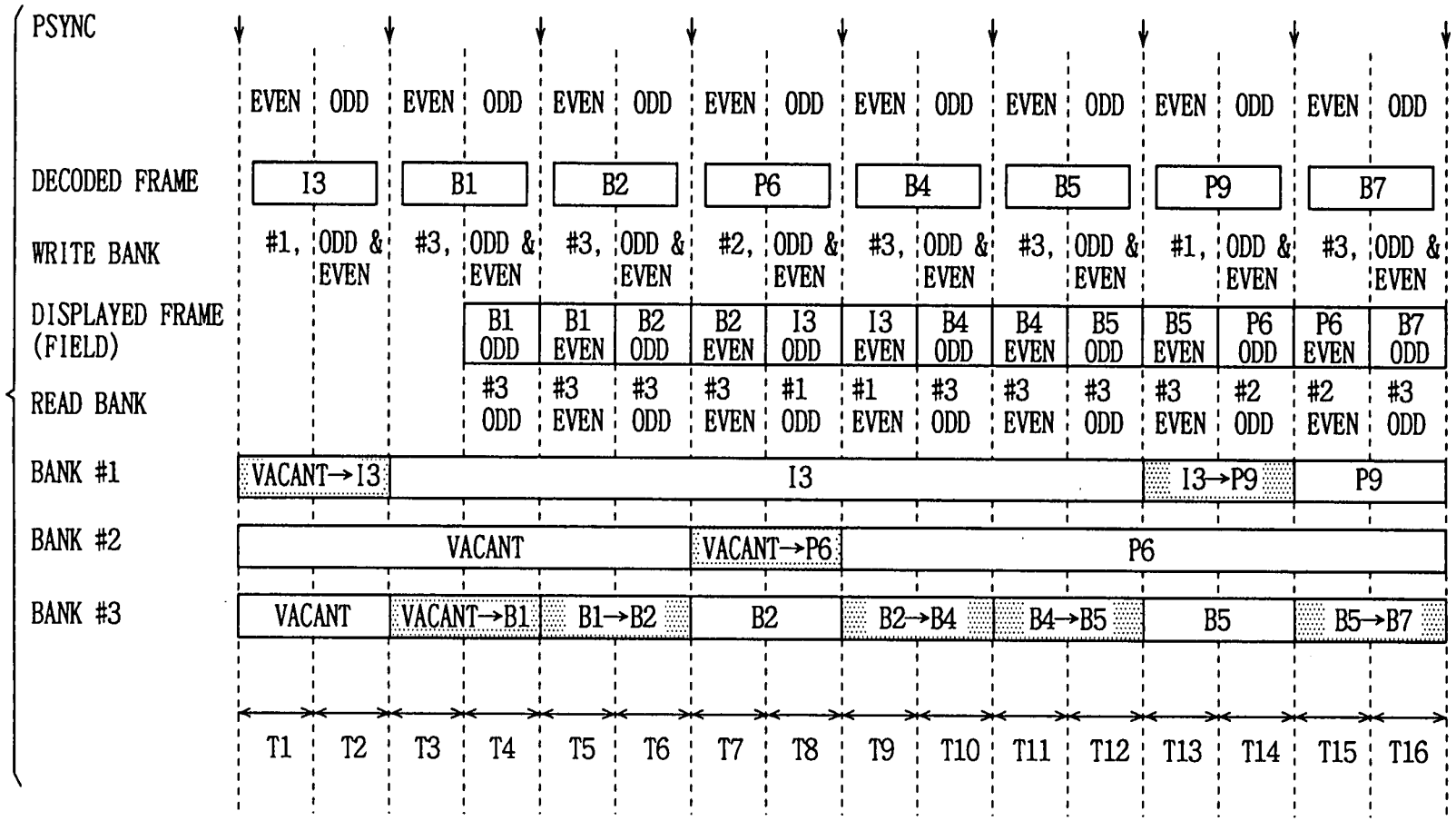


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FIG. 5

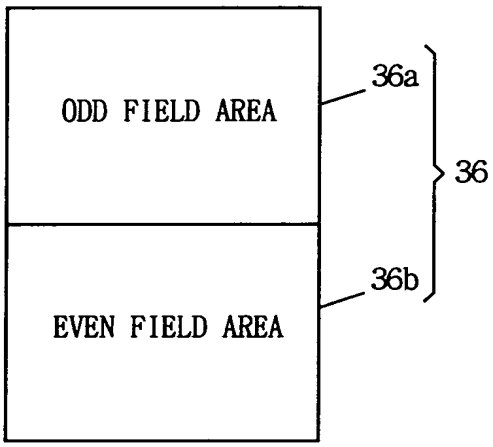


FIG. 6A

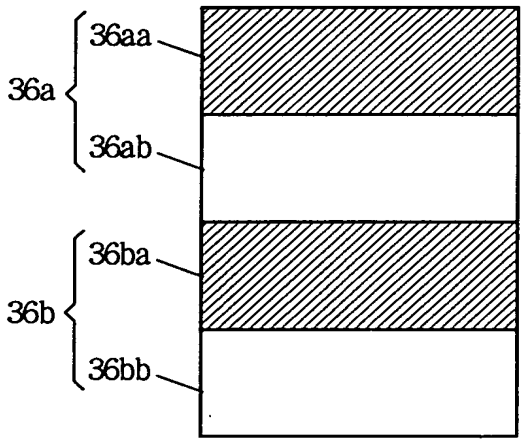


FIG. 6B

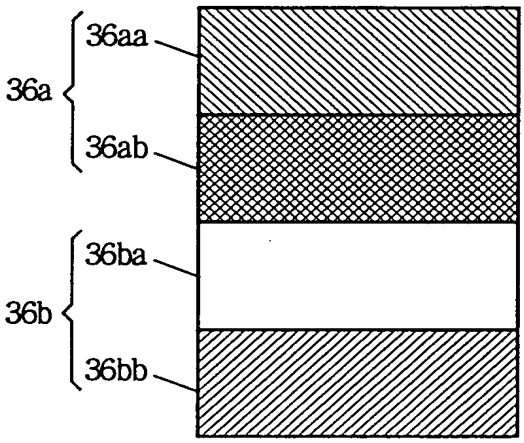


FIG. 7A

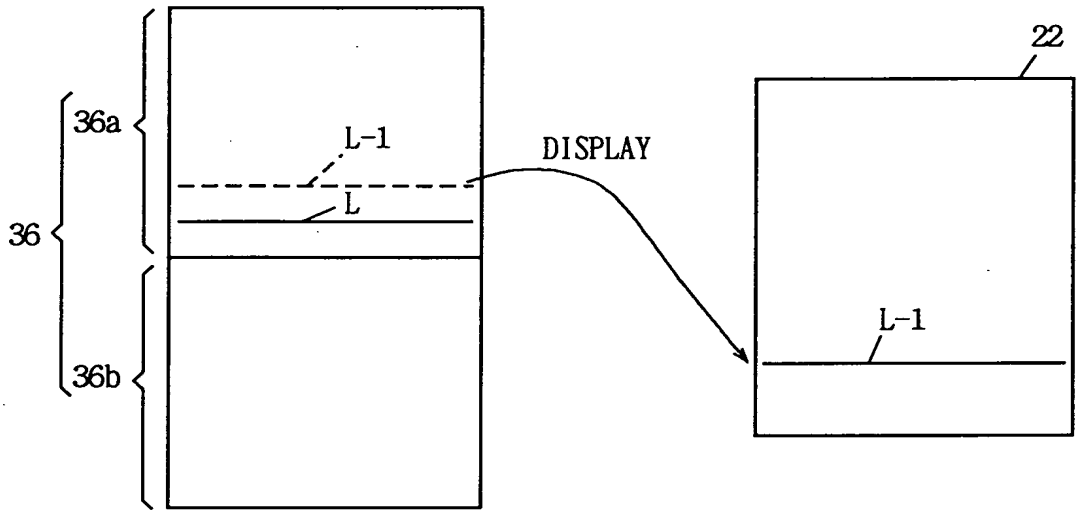


FIG. 7B

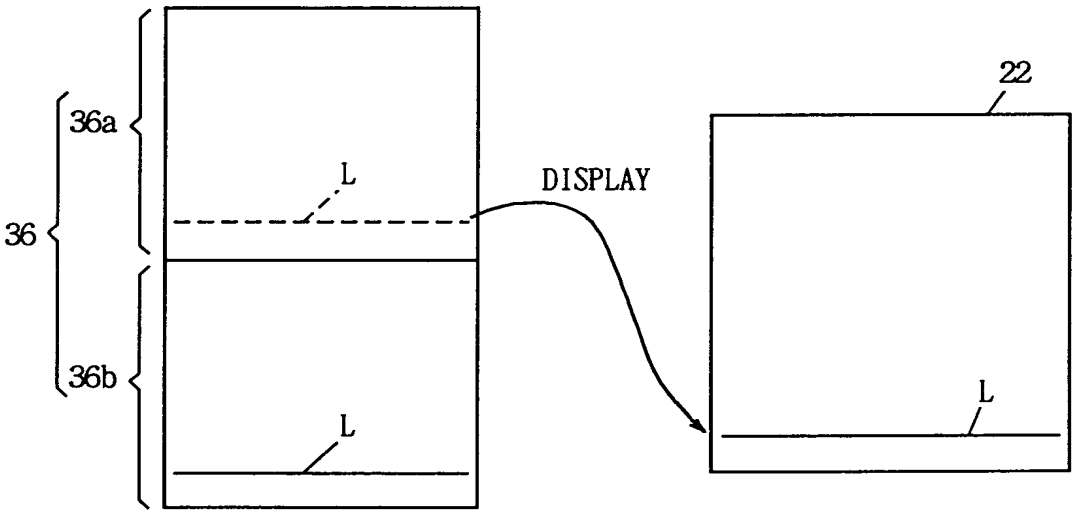


FIG. 8A

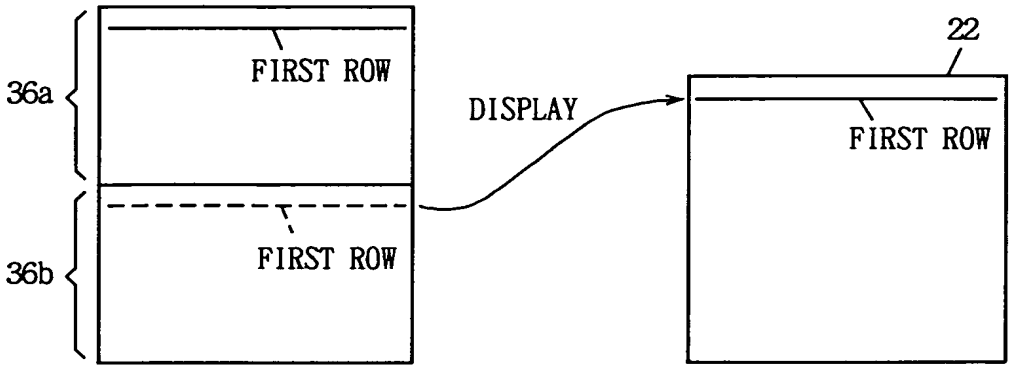


FIG. 8B

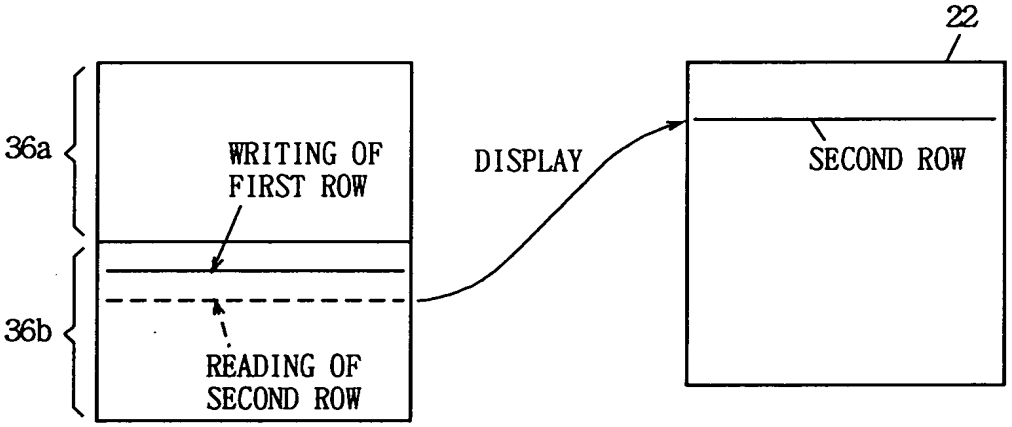


FIG. 8C

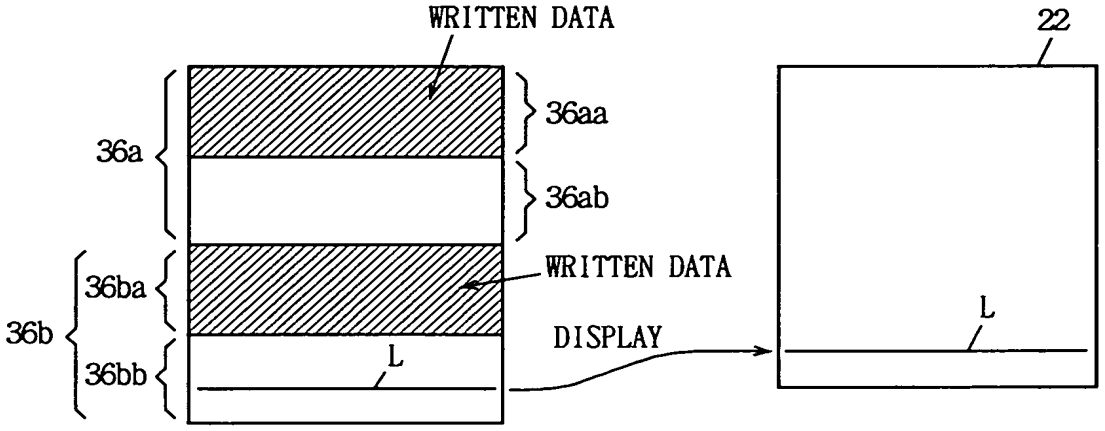


FIG. 9

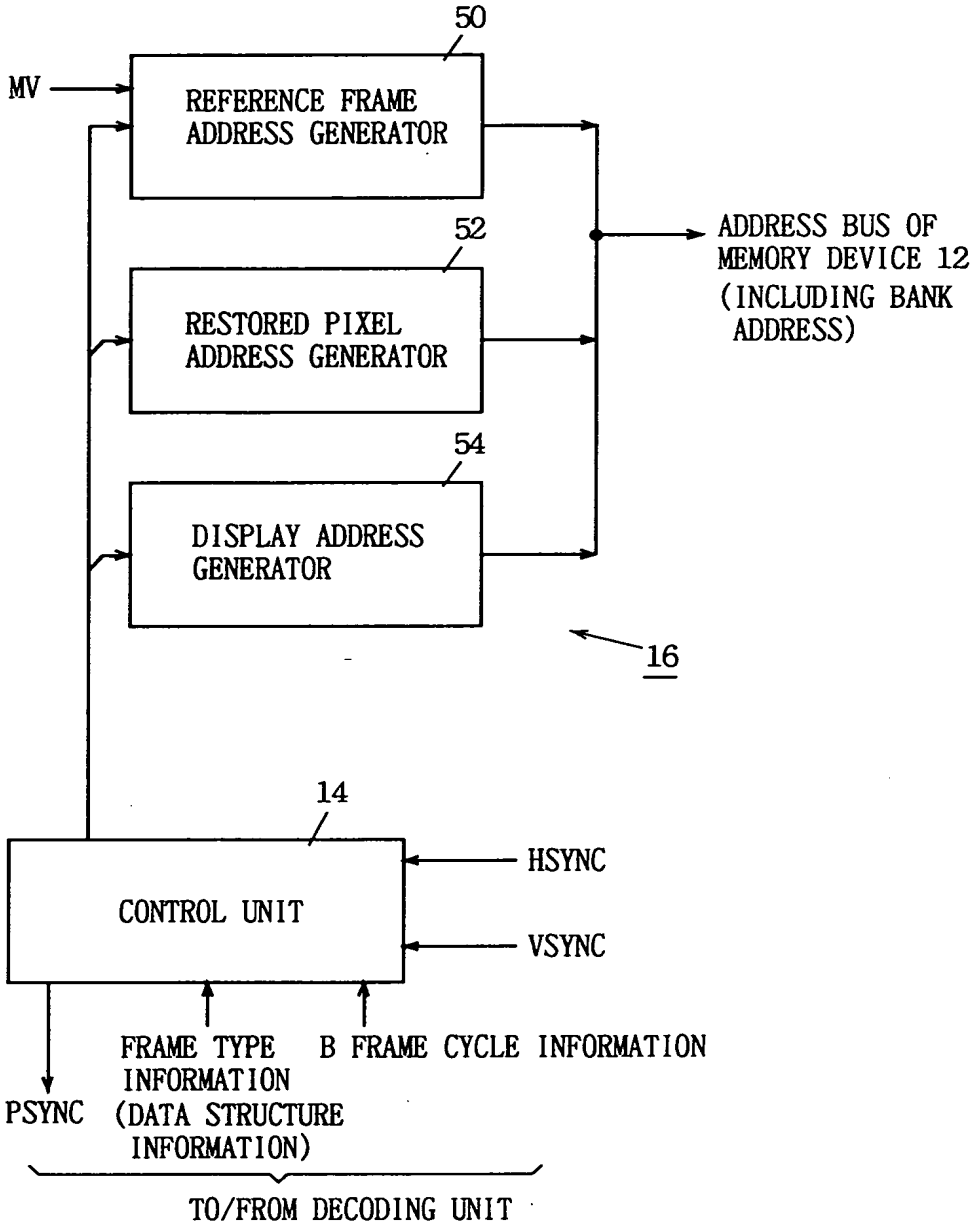

50
MV
REFERENCE FRAME ADDRESS GENERATOR
52
RESTORED PIXEL ADDRESS GENERATOR
54
DISPLAY ADDRESS GENERATOR
ADDRESS BUS OF MEMORY DEVICE 12 (INCLUDING BANK ADDRESS)
16
14
CONTROL UNIT
HSYNC
VSYNC
PSYNC
FRAME TYPE INFORMATION (DATA STRUCTURE INFORMATION)
B FRAME CYCLE INFORMATION
TO/FROM DECODING UNIT

FIG. 10

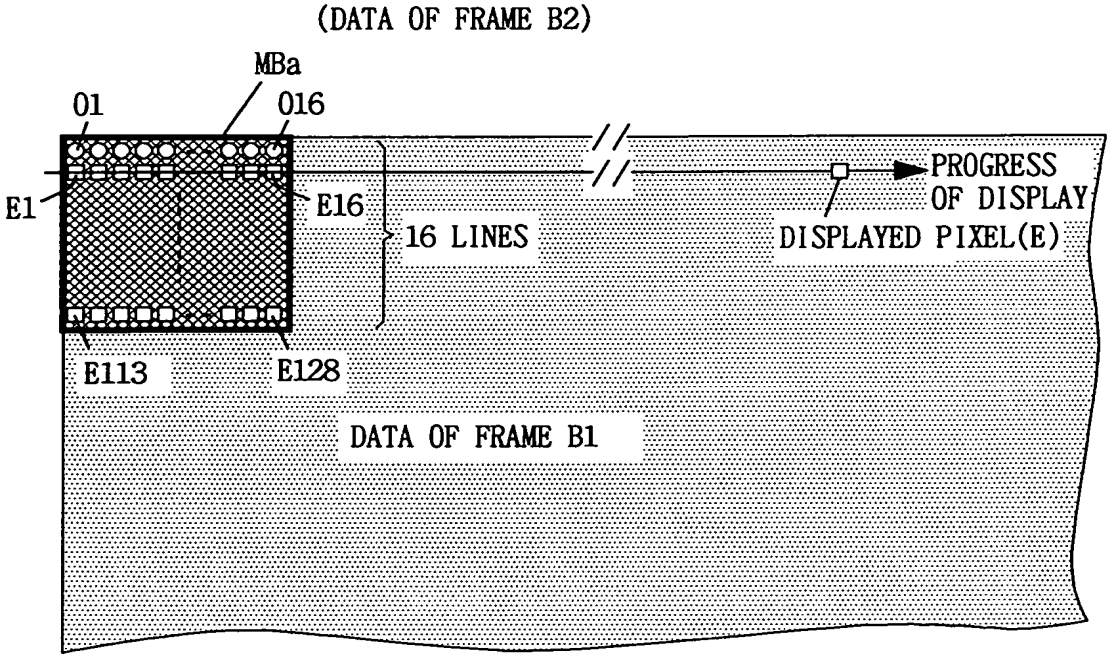

(DATA OF FRAME B2)
MBa
01
016
E1
E16
16 LINES
PROGRESS
OF DISPLAY
DISPLAYED PIXEL(E)
E113
E128
DATA OF FRAME B1

FIG. 11

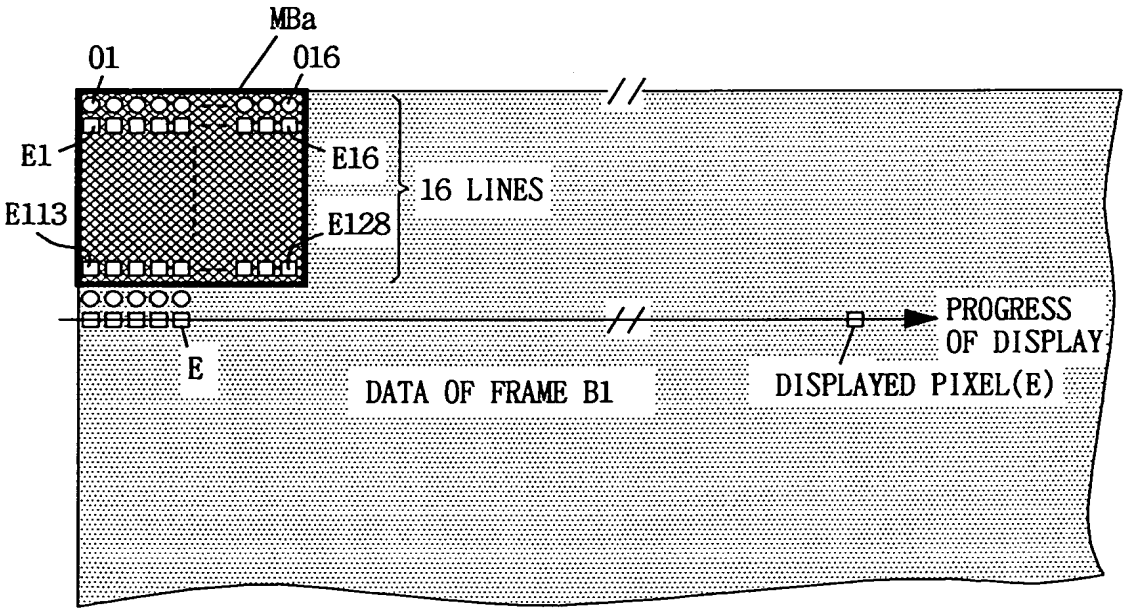

MBa
01
016
E1
E16
16 LINES
E113
E128
E
PROGRESS
OF DISPLAY
DATA OF FRAME B1
DISPLAYED PIXEL(E)

FIG. 12

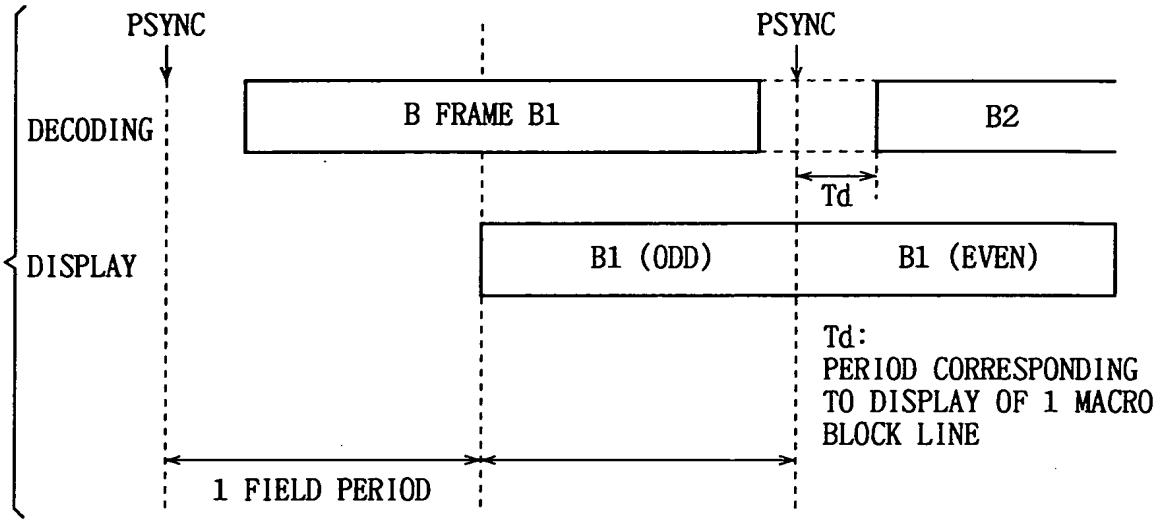

PSYNC
PSYNC
DECODING
B FRAME B1
B2
Td
DISPLAY
B1 (ODD)
B1 (EVEN)
Td:
PERIOD CORRESPONDING
TO DISPLAY OF 1 MACRO
BLOCK LINE
1 FIELD PERIOD

FIG. 13

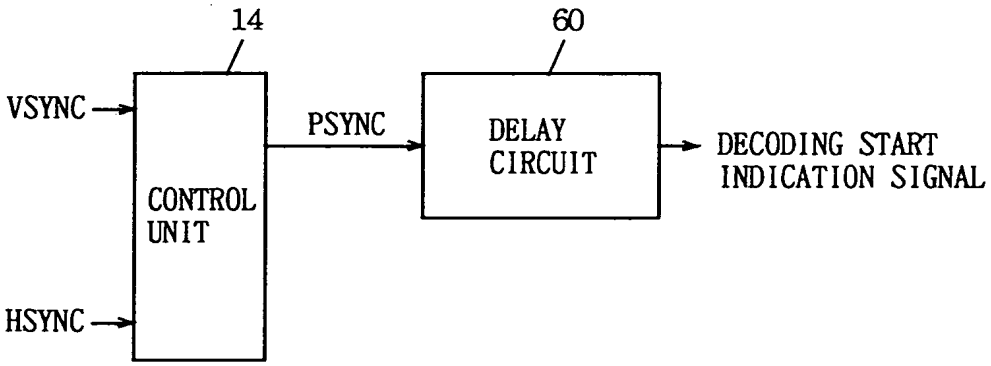

14
60
VSYNC
PSYNC
DELAY
CIRCUIT
DECODING START
INDICATION SIGNAL
CONTROL
UNIT
HSYNC

FIG. 14

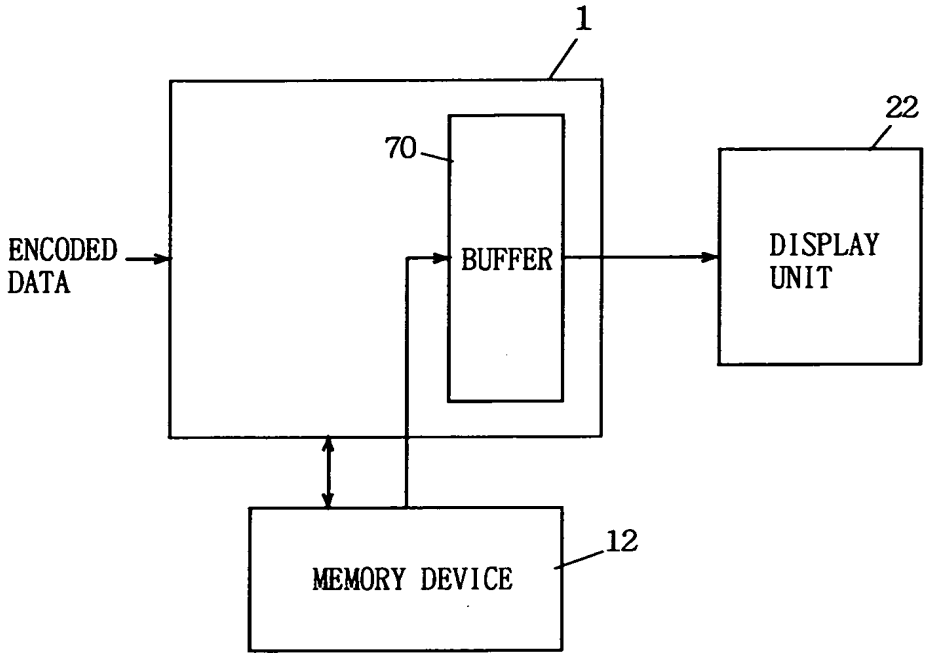
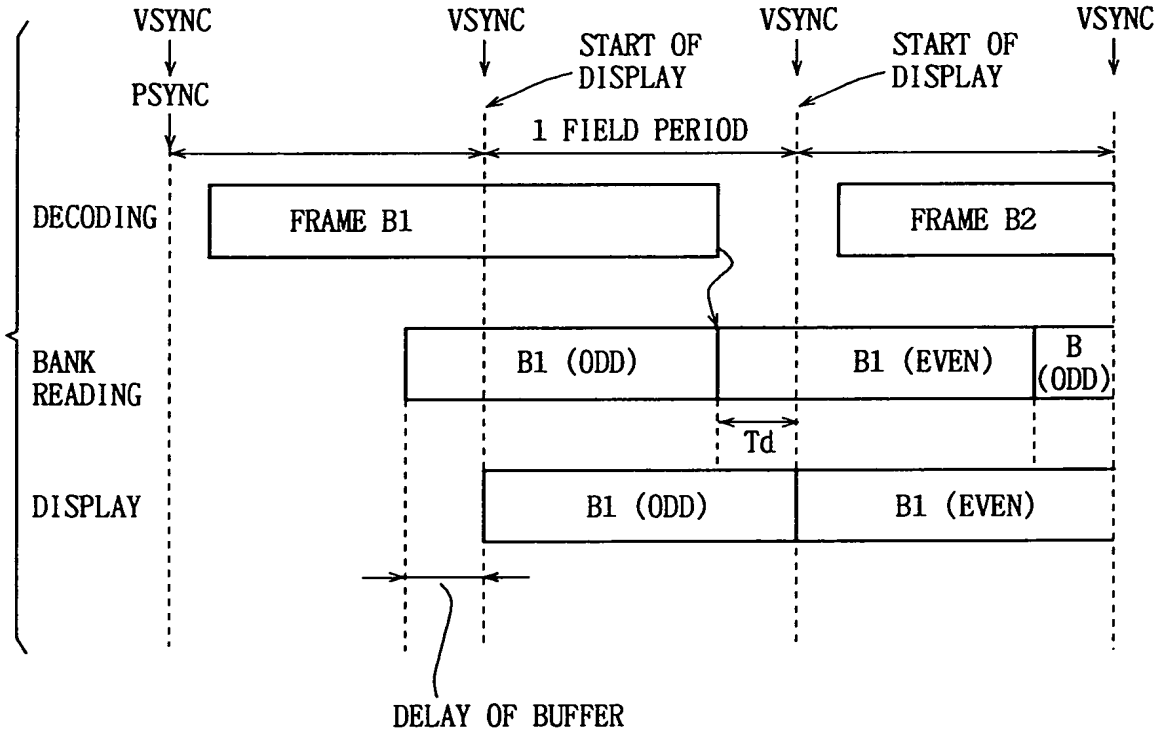

1
70
22
ENCODED DATA
BUFFER
DISPLAY UNIT
MEMORY DEVICE
12

FIG. 15


VSYNC
PSYNC
VSYNC
START OF DISPLAY
VSYNC
START OF DISPLAY
VSYNC
1 FIELD PERIOD
DECODING
FRAME B1
FRAME B2
BANK READING
B1 (ODD)
B1 (EVEN)
B (ODD)
Td
DISPLAY
B1 (ODD)
B1 (EVEN)
DELAY OF BUFFER

O.G. FIG.
BY
CLASS SUBCLASS
EXAMINER

FIG. 16A PRIOR ART

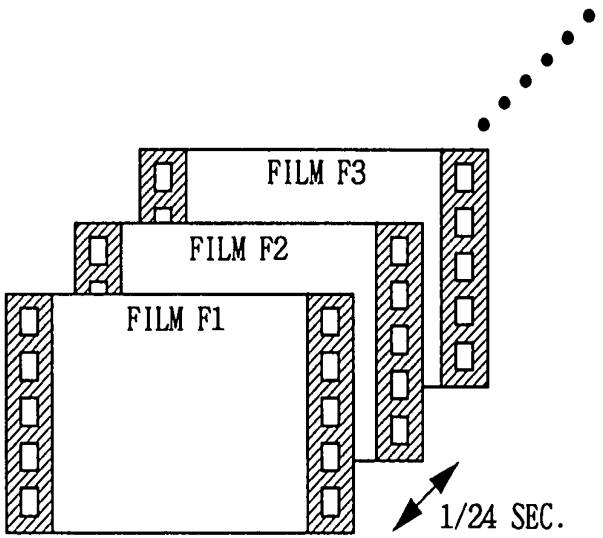
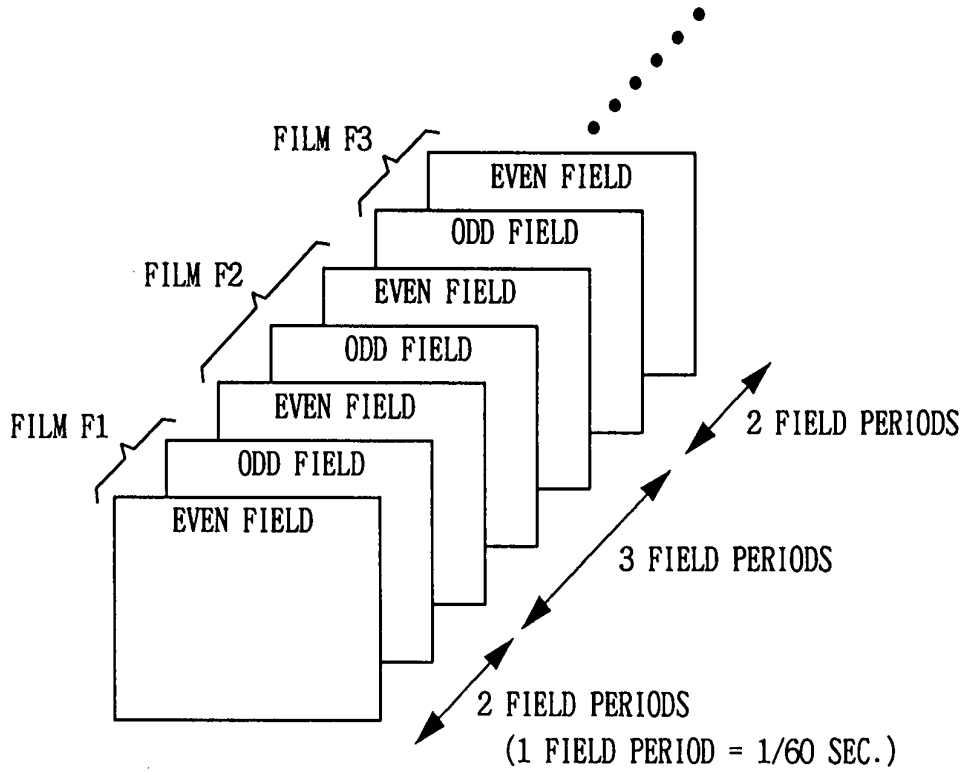


FIG. 16B PRIOR ART



CINEFILM (24 FRAMES/SEC.) → DISPLAYED PICTURE (60 FIELDS/SEC.)

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O.G. FIG.
BY
CLASS SUBCLASS
EXAMINER

FIG. 17

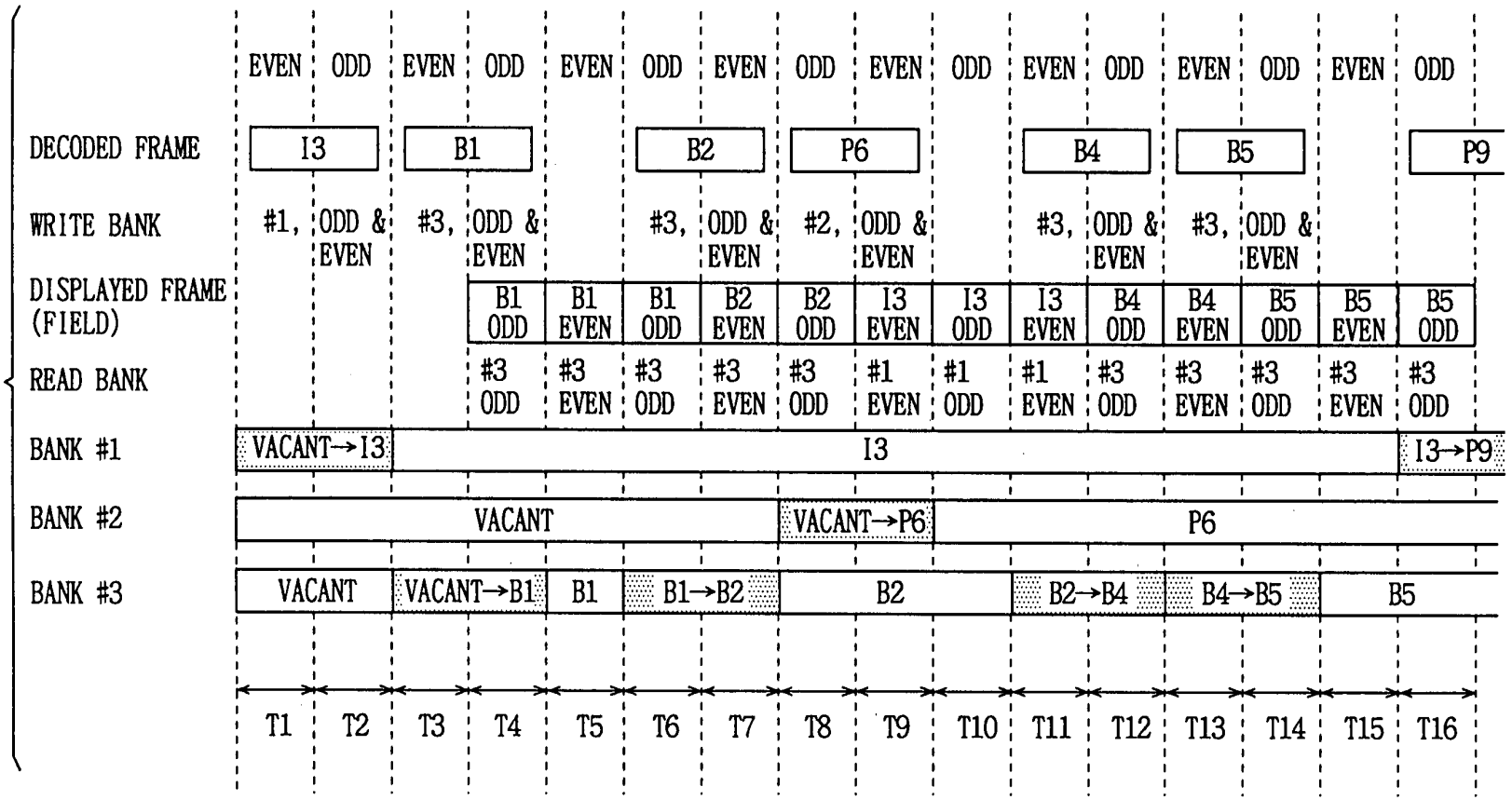

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FIG. 18

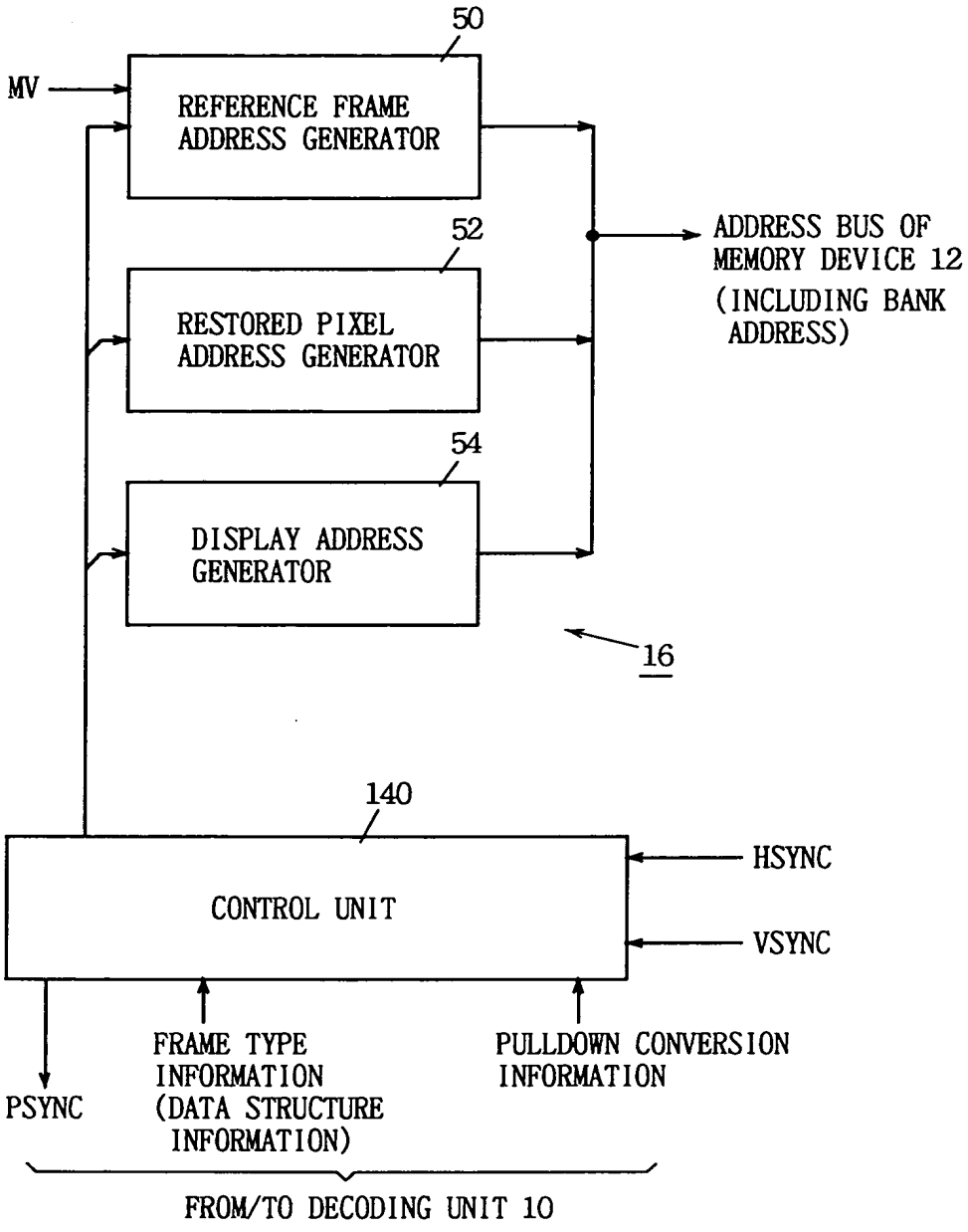

50
MV
REFERENCE FRAME ADDRESS GENERATOR
52
RESTORED PIXEL ADDRESS GENERATOR
54
DISPLAY ADDRESS GENERATOR
ADDRESS BUS OF MEMORY DEVICE 12 (INCLUDING BANK ADDRESS)
16
140
CONTROL UNIT
HSYNC
VSYNC
PSYNC
FRAME TYPE INFORMATION (DATA STRUCTURE INFORMATION)
PULLDOWN CONVERSION INFORMATION
FROM/TO DECODING UNIT 10

FIG. 19

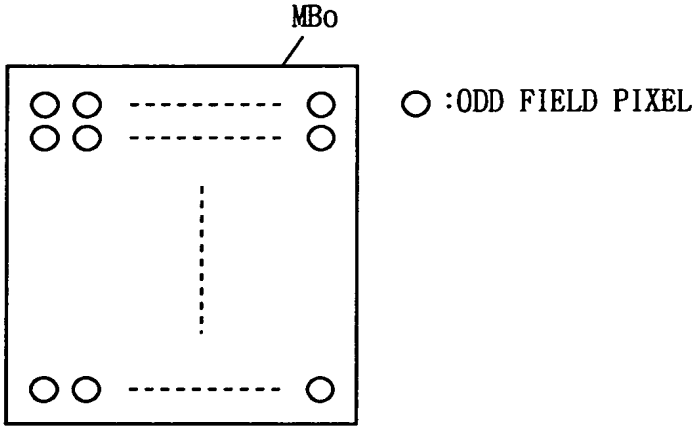
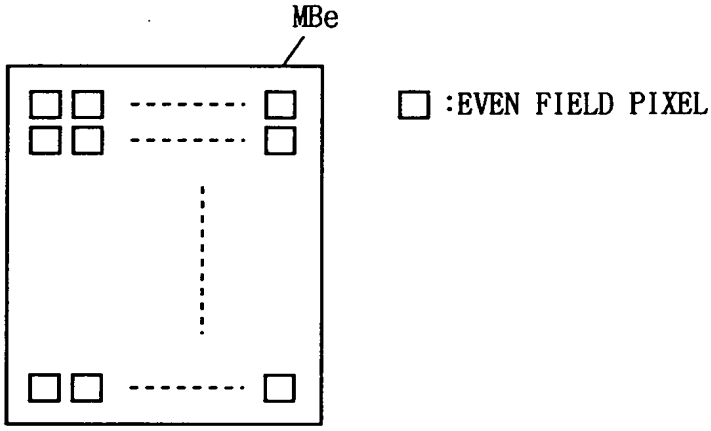


FIG. 20



O.G. Fig.
CLAS. SUBCLASS
BY LAFIGMAN

FIG. 21

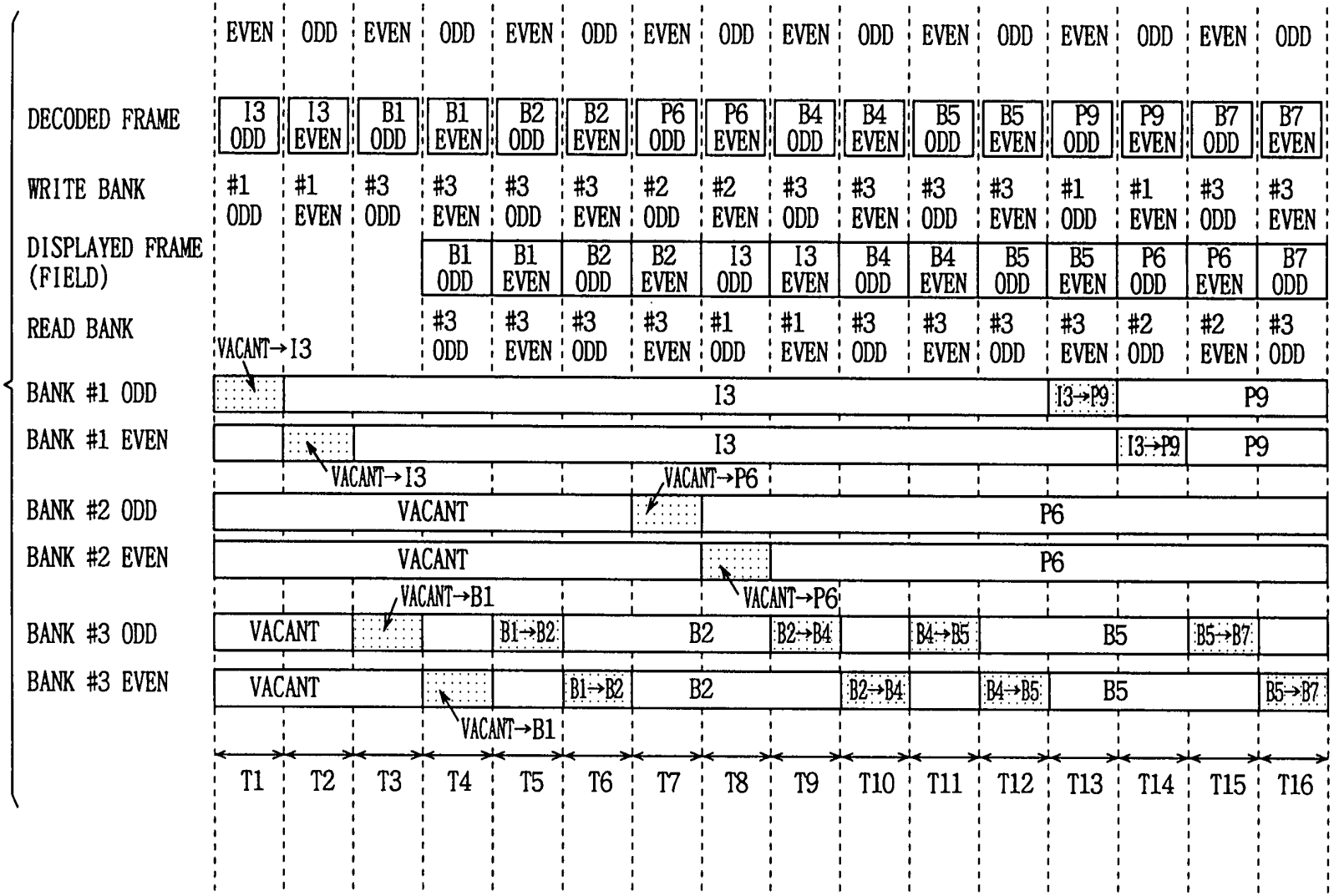


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FIG. 22A

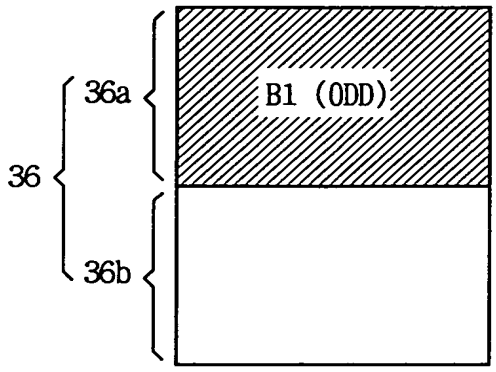


FIG. 22B

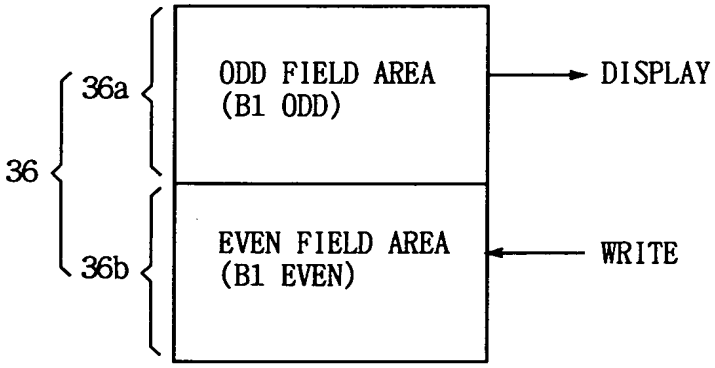


FIG. 22C

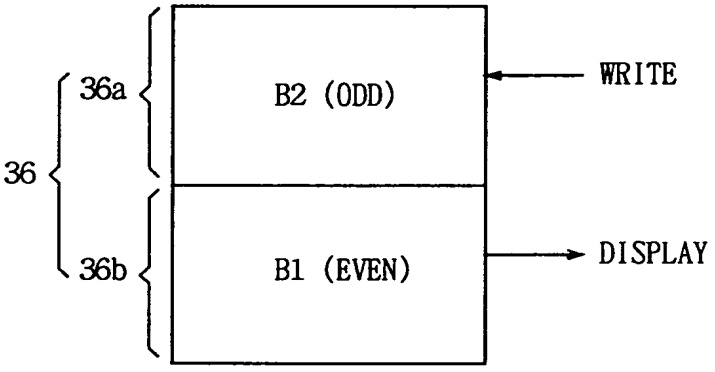


FIG. 23

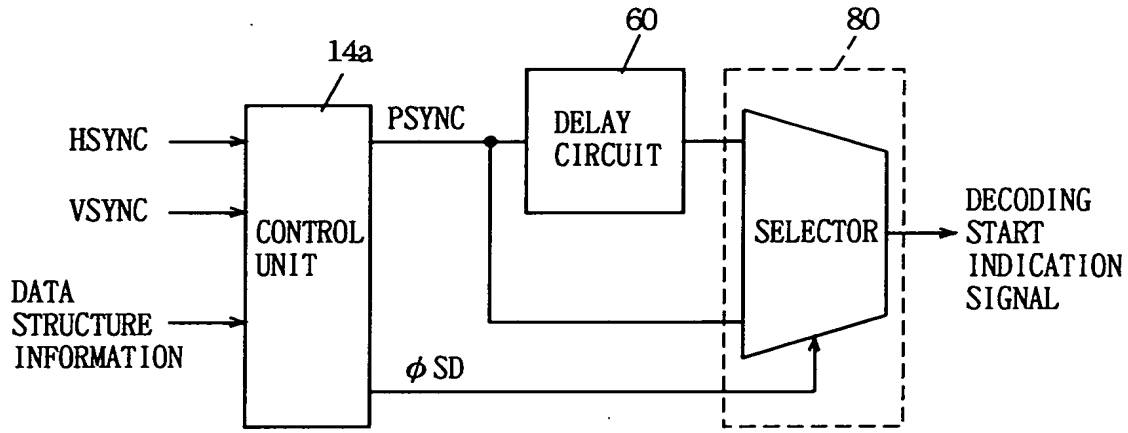
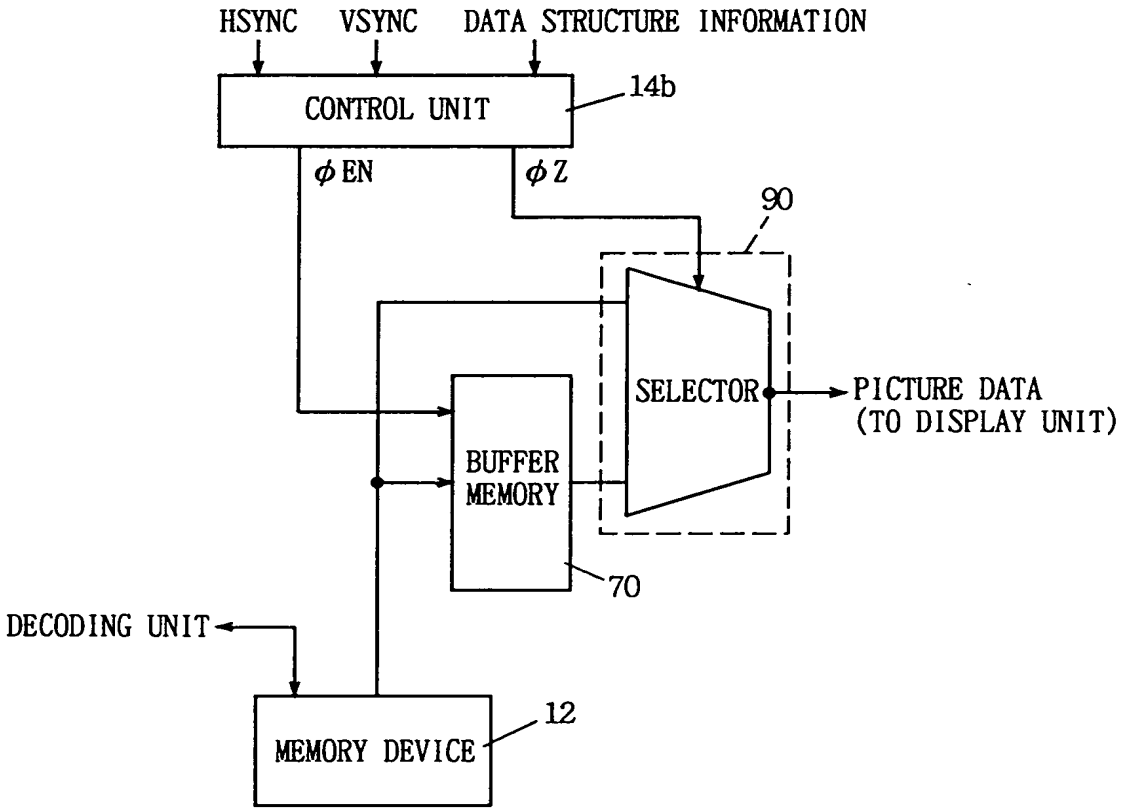

60
80
14a
HSYNC
VSYNC
DATA
STRUCTURE
INFORMATION
CONTROL
UNIT
PSYNC
DELAY
CIRCUIT
SELECTOR
DECODING
START
INDICATION
SIGNAL
φSD

FIG. 24


HSYNC
VSYNC
DATA STRUCTURE INFORMATION
CONTROL UNIT
14b
φEN
φZ
90
SELECTOR
PICTURE DATA
(TO DISPLAY UNIT)
BUFFER
MEMORY
70
DECODING UNIT
MEMORY DEVICE
12

O.G. FIG.
BY
CLASS SUBCLASS
EXAMINER

FIG. 25

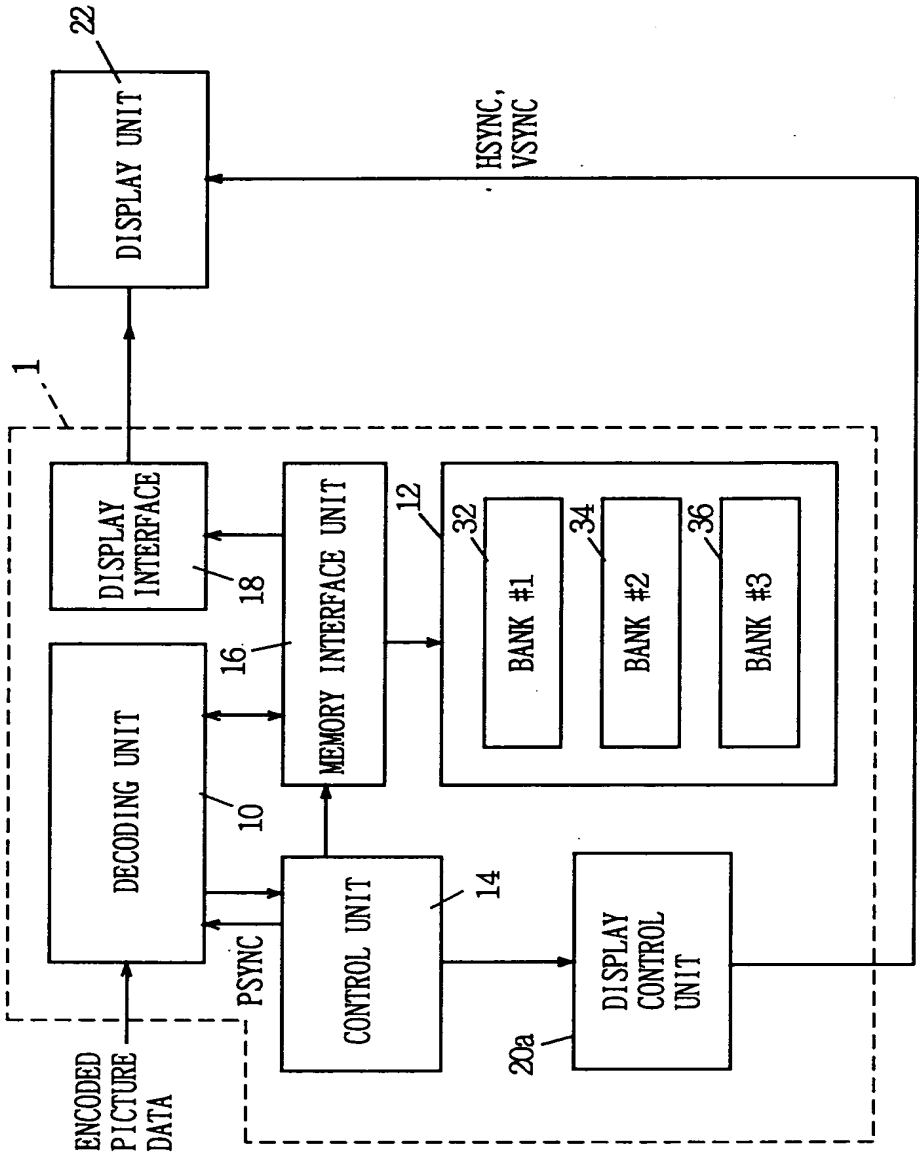
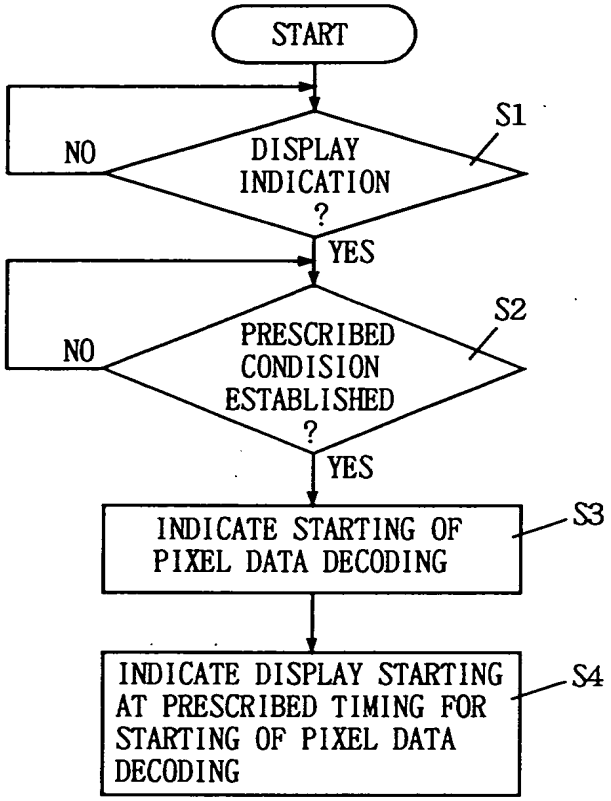


FIG. 26



O.G. FIG.
CLASS SUBCLASS
BY DRAFTSMAN

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O.G. FIG.
CLAS.
DRAFTSMAN

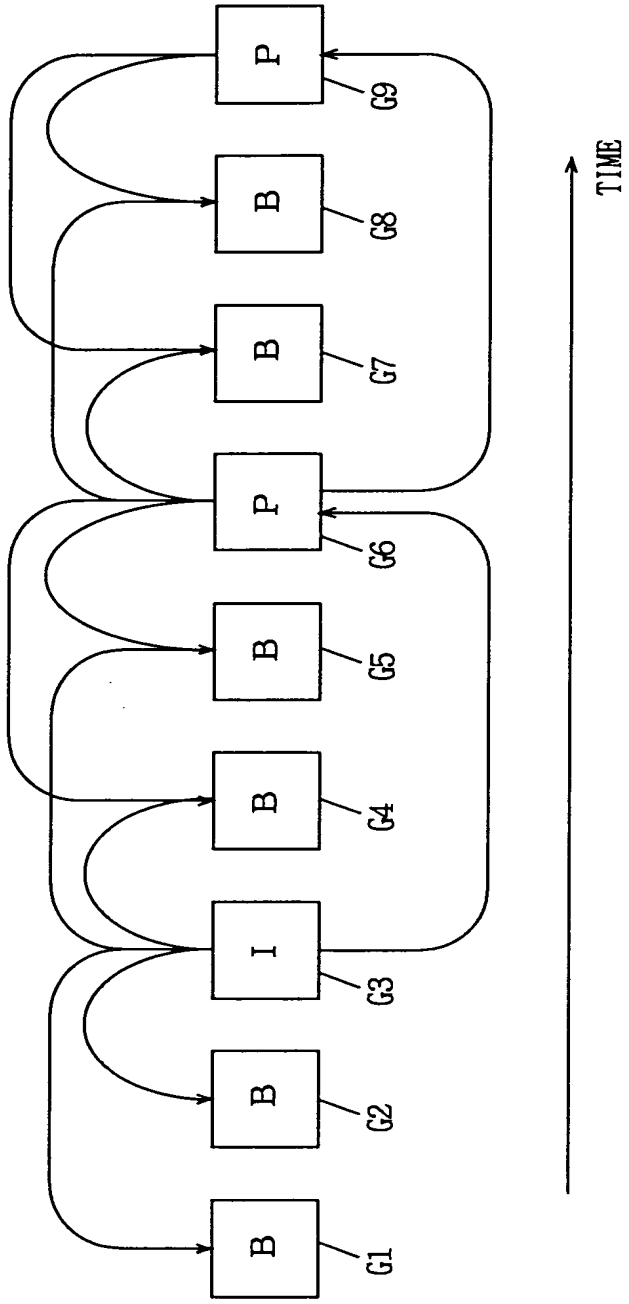
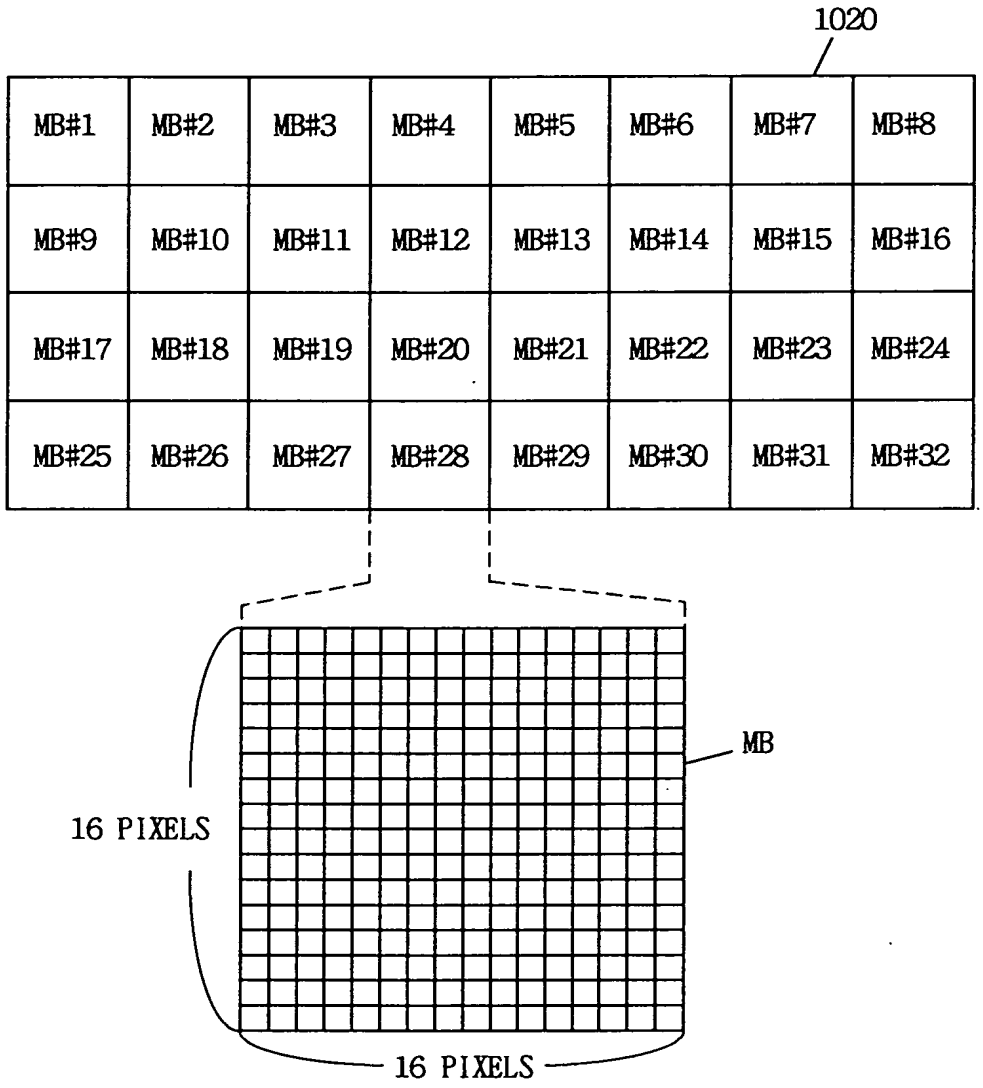


FIG. 27 PRIOR ART

FIG. 28 PRIOR ART



O.G. FIG.
BY
CLASS SUB-CLASS
FAITSMAN

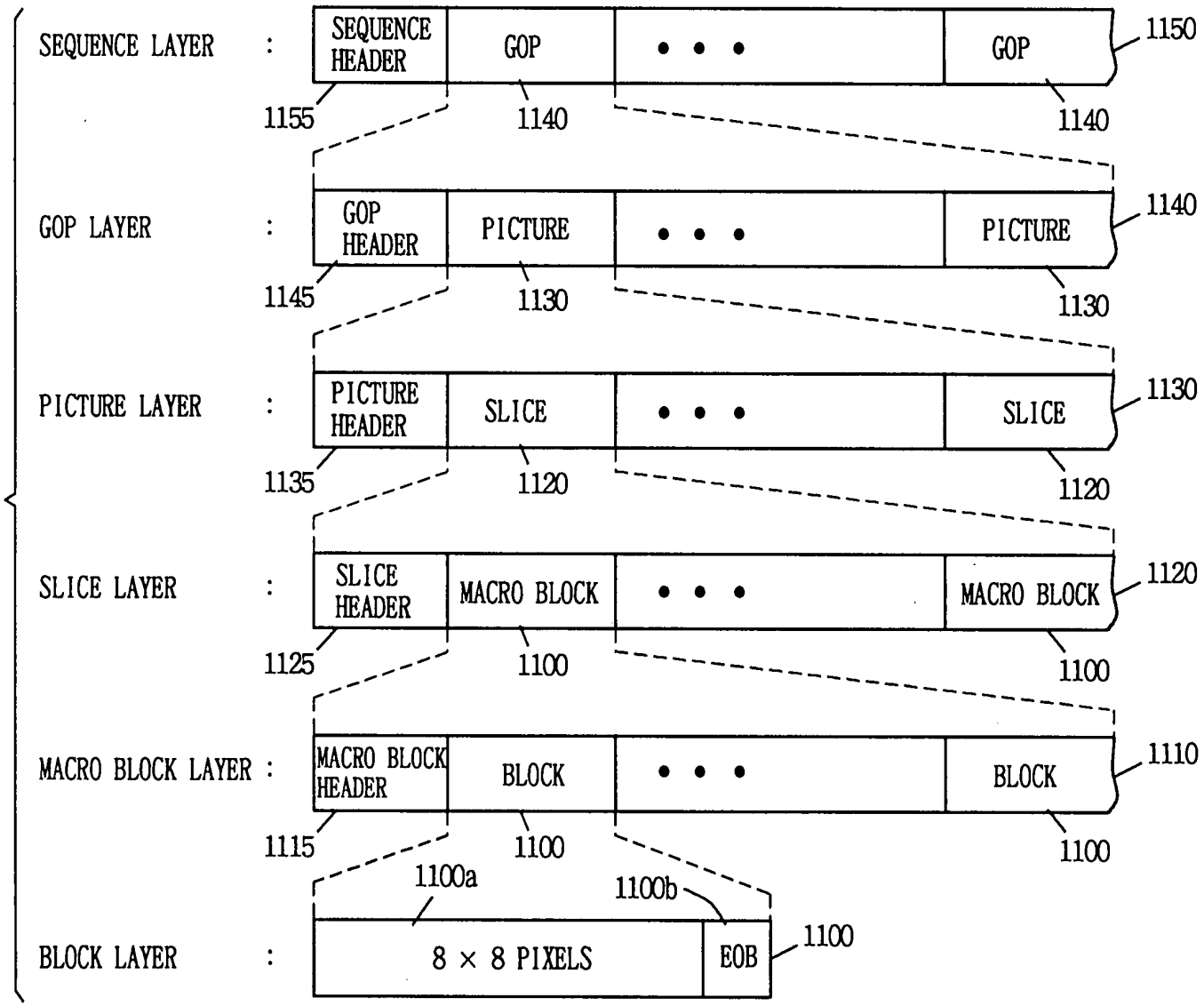


FIG. 29
PRIOR ART

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O.G. PRINT
CLASS SUBCLASS
BY EXAMINER

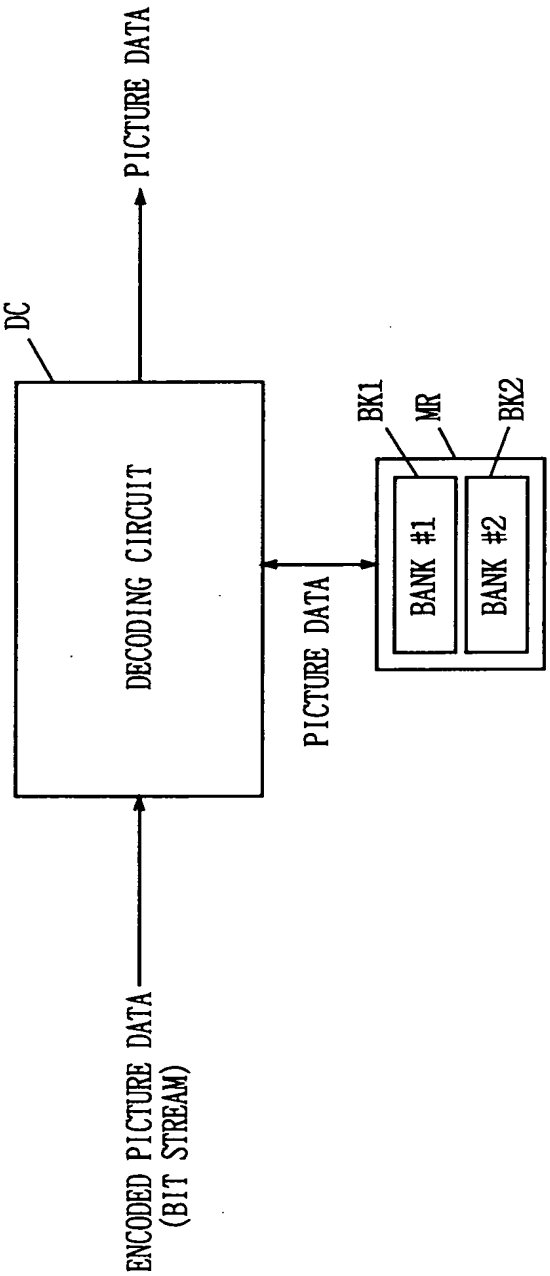

FIG. 30 PRIOR ART

O.G.
BY
CLAS.
CLASS
AFTSMAN

FIG. 31A PRIOR ART

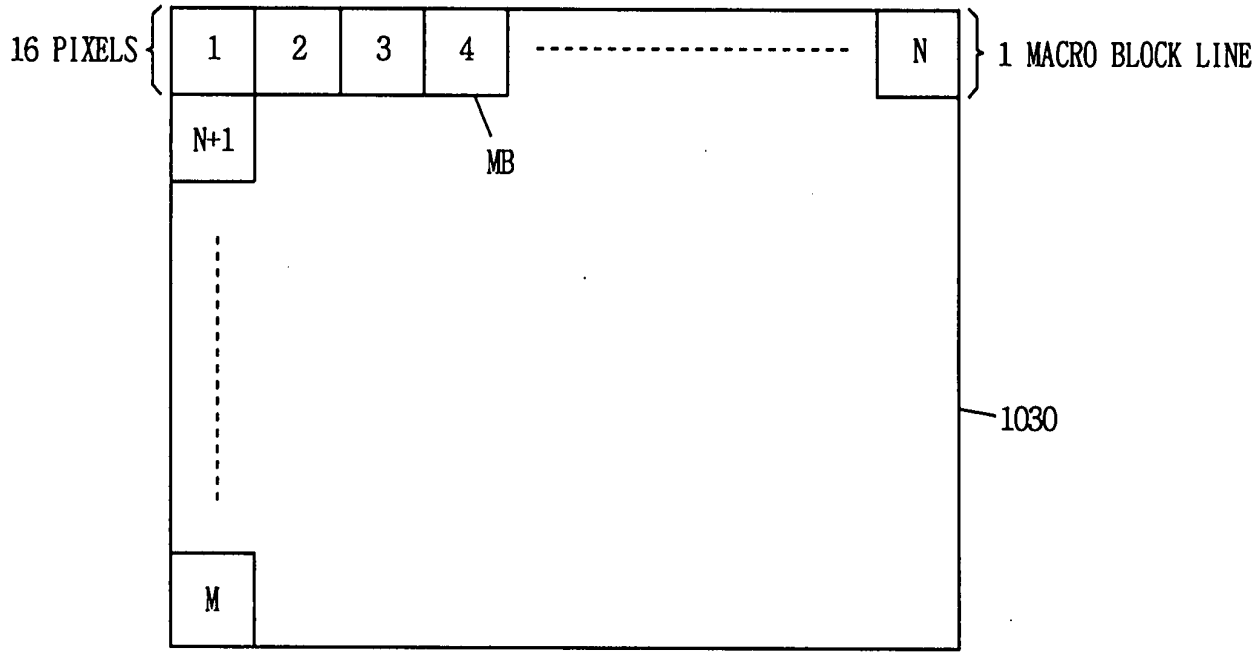

FIG. 31B PRIOR ART

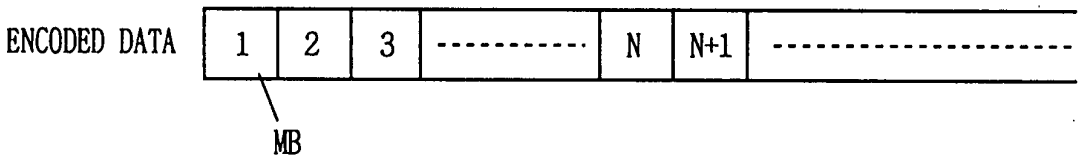

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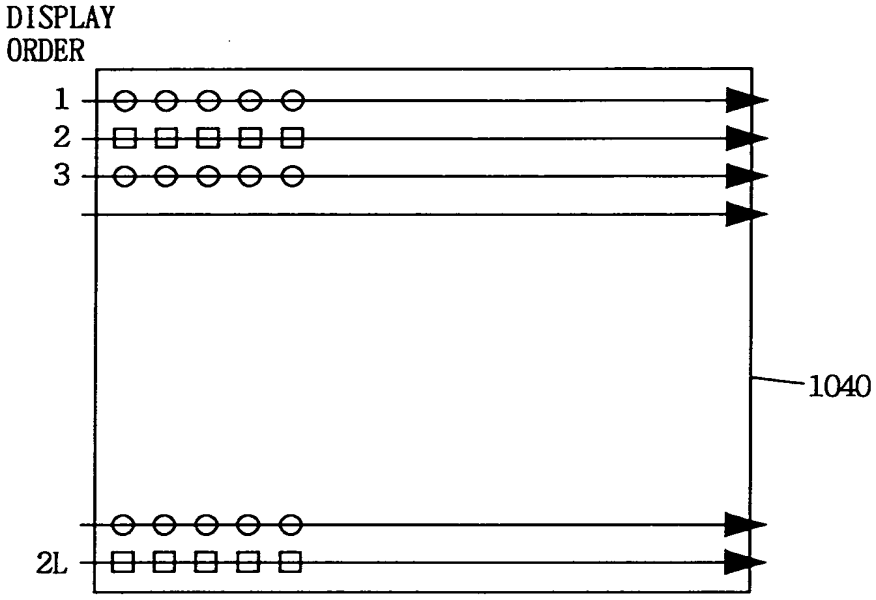
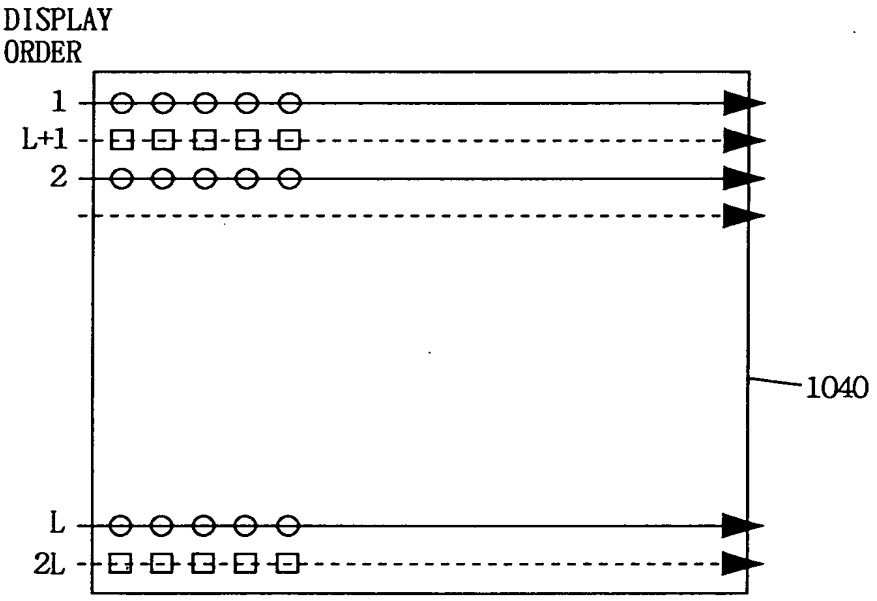
FIG. 32 PRIOR ART



NON-INTERLACE DISPLAY

FIG. 33 PRIOR ART



INTERLACE DISPLAY

O.G. CLASS

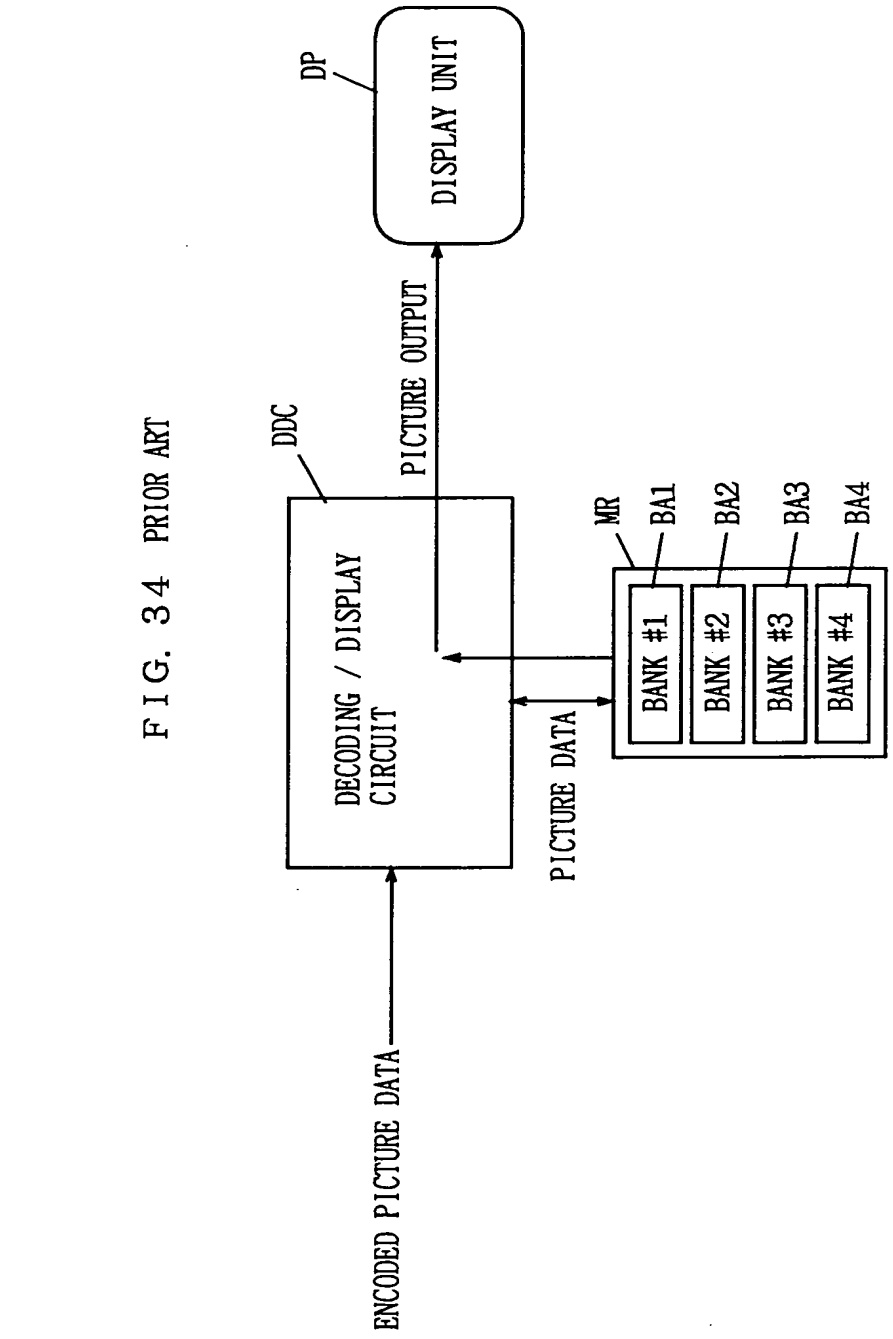
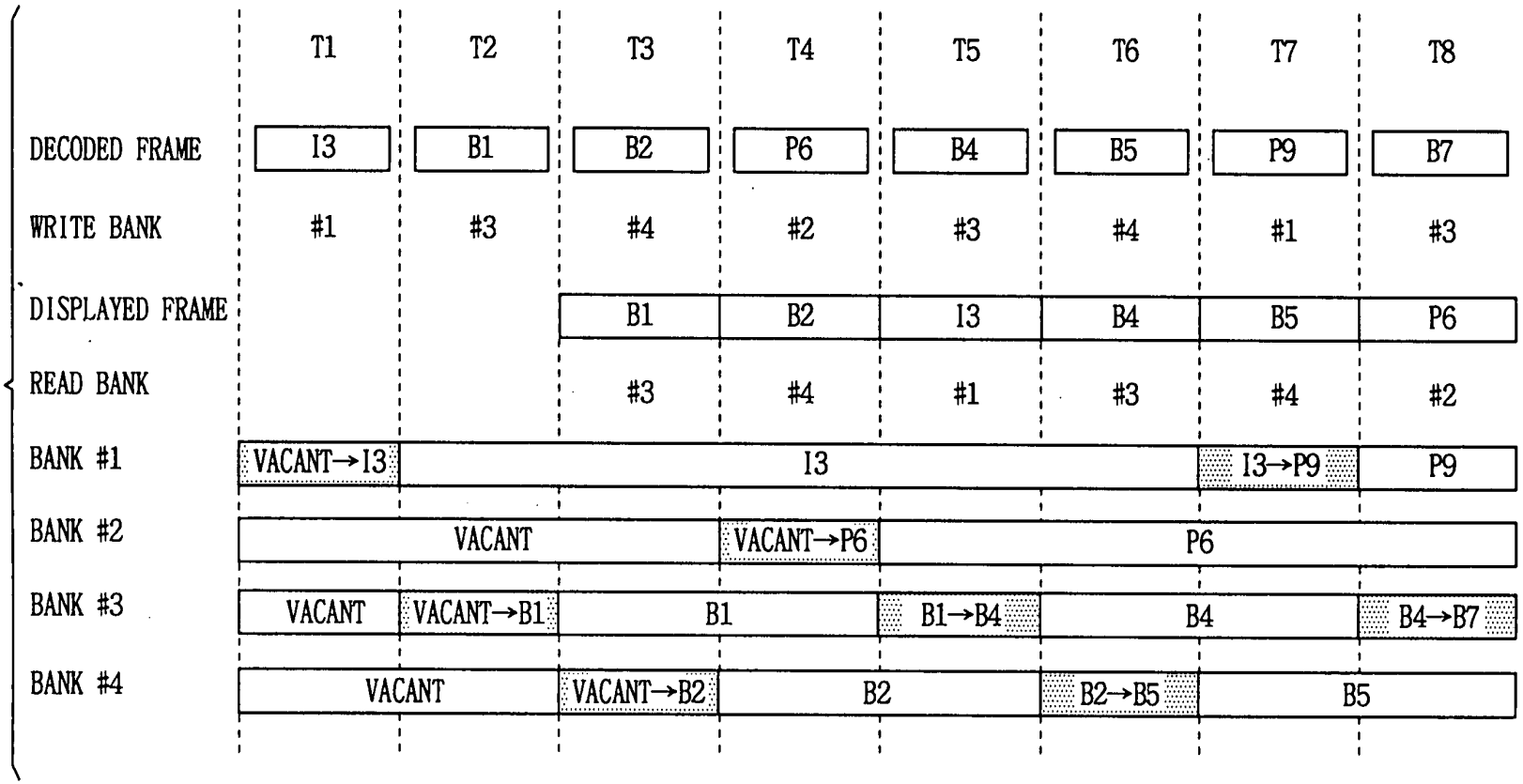


FIG. 34 PRIOR ART

O.G. FIG.
BY
CLASS SUBCLASS
BAETSMAN

FIG. 35 PRIOR ART



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